Table 10 Monolithic Integrated Circuit Screening Requirements

Inspection/ Test	Methods	MIL-STD-883 Conditions and Requirements	Grade 1	Grade 2
1. Wafer Acceptance	5007		X	
2. Nondestructive Bond Pull	2023		X	
3. Internal Visual	2010	Condition A or B (Note 1).	X	X
4. Temperature Cycling	1010	Condition C (-65 °C to + 150 °C) in N_2 atmosphere. 20 cycles.	X	X
5. Constant Acceleration	2001	Condition E (Note 2). Y_1 orientation only.	X	X
6. PIND	2020	Condition A.	X	X
7. Radiographic	2012	1 view for Quad Flat Pack and Leadless Chip Carrier. 2 views for other package styles. Can be performed at any time after PIND.	X	
8. Serialization			X	
9. Initial Electrical Measurements		Read and record delta parameters per Table 10A.	X	X
10. Burn-In (Note 3)	1015	Condition C and/or D per Table 10A. Duration (hours) for Static/Dynamic burn-in as required in Table 10A.	X 72/240	X 160
11. Final Electrical Measurements		Per Table 10A.	X	X
12. Calculate Deltas		See Table 10A.	X	
13. Percent Defective Allowable		PDA applies to delta, selected DC and functional tests at test temperature of 25 °C.	Δ+DC ≤5% Functional ≤ 3%	DC ≤10%
14. Hermetic Seal a. Fine Leak b. Gross Leak	1014	 Condition A or B. Condition C.	X	X
15. External Visual	2009	3 X to 10X.	X	X

Notes:

1. Destructive Physical Analysis may be performed to the requirements of S311-M-70 in lieu of internal visual for devices used in Grades 2 applications.
2. For packages having a cavity perimeter of 2 inches or more in total length, or having a mass greater than 5 grams, test condition D can be used.
3. A dynamic burn-in or a static burn-in shall be performed in accordance with Table 10A. Static and dynamic burn-in is required for Grade 1 parts when so indicated in Table 10A. A dynamic or static burn-in shall be performed in accordance with Table 10A for Grade 2 parts.

Table 10A Burn-In and Electrical Measurement Requirements for Monolithic ICs (Page 1 of 4)

IC Type	Required Burn-In (Note 4)		Delta	Electrical Measurements (Notes 1, 2, 3)
	Static (Condition C)	**Dynamic (Condition D)**		
Digital Bipolar & Digital MOS/ BiCMOS: (Note 6) LOGIC (Gates, Buffers, Flip-Flops, Multiplexers, Registers and Counters) RAMs FIFOs Microprocessors Interface Peripherals ASICs FPGA, PROM, PLA (Note 5)	Not required for Digital Bipolar Technology. Required for Digital MOS Technology. $T_A \geq 125$ °C V_{in}= V_{DD} across one-half input pins and V_{SS} across the remaining inputs. V_{out}= 0.5 V_{DD} through R_L	Required for both technologies. $T_A \geq 125$ °C V_{in} = Square wave, 50% Duty Cycle to input pins and control pins. Frequency= 100 Hz to 1 Mhz. V_{out} = V_{CC} /2 or V_{DD}/2 through R_L.	ΔI_{CC} or ΔI_{DD}	**DC**: V_{IC}, V_{OH}, V_{OL}, I_{CC}(I_{EE}), I_{IL}, I_{IH}, $I_{DD,}$ I_{OZL}, I_{OZH}, I_{OS} **AC:** T_{PLH}, T_{PHL}, T_{TLH}, T_{THL}, T_{PZH}, T_{PHZ}, T_{PLZ}, T_{PZL}, T_A, T_S, T_H **Functional Tests:** a) for simple logic devices,verify truth table b) for complex logic devices such as ASIC, FPGA, microprocessors, functional testing includes fault coverage calculations required per Mil-Std-883, Method 5012. c) for PROMs, check fuse map; for RAMs, perform pattern sensitive tests such as March, galpat, etc.
Linear MOS, Bipolar, and Bi-FET: (Note 7) Op-Amp, Instrument Amplifiers, S/H, and Comparator	$T_A \geq 125$ °C V_{out}= Terminated to ground through R_L	$T_A \geq 125$ °C V_{in}= Square wave or sinewave F= 10Hz to 100 KHz, 50% duty cycle V_{out}= Terminated to ground through R_L	ΔI_{IB} ΔI_{IO} ΔV_{IO}	**DC**: I_{CC}, I_{EE}, I_{IO}, V_{IO}, V_{OPP}, A_V, CMRR, PSRR **AC**: Slew rate

See notes on page C-35.

Table 10A Burn-In and Electrical Measurement Requirements for Monolithic ICs (Page 2 of 4)

IC Type	Required Burn-In (Note 4)		Delta	Electrical Measurement (Notes 1, 2, 3)
	Static (Condition C)	**Dynamic (Condition D)**		
Linear MOS, Bipolar and JFET: (Note 7) Line Drivers and Receivers	$T_A \geq 125$ °C $V_{in} = V_{DD}$ max across one-half input pins and V_{SS} across the remaining inputs.	$T_A \geq 125$ °C V_{in}= Square wave at a specified Vdc $V_{out} = V_{CC}$ through R_L	ΔI_{CC} ΔI_{IH}	**DC**: V_{OH}, V_{OL}, I_{CC}, I_{IL}, I_{IH}, I_{OS} **AC**: T_{PLH}, T_{PHL}, T_{TLH}, T_{THL} **Functional Test**: verify truth table
Linear MOS, Bi-FET, and Bipolar: (Note 6) Analog Switches and Multiplexers	$T_A \geq 125$ °C $V_{in} = V_{DD}$ max across one-half of inputs and V_{SS} across the other remaining inputs. $V_{out} = \pm V_{CC}$ through R_L	$T_A \geq 125$ °C V_{in}= Square wave F= 100 Khz and 50% duty cycle $V_{out} = \pm V_{CC}$ through R_L	I_{CC} $I_{D(OFF)}$ $I_{S(OFF)}$ $R_{(ON)}$	**DC**: I_{CC}, $I_{D(ON)}$, $R_{(ON)}$, $I_{D(OFF)}$, $I_{S(ON)}$, $I_{S(OFF)}$ **AC**: $T_{(ON)}$, $T_{(OFF)}$ break- before- make- time
Linear Bipolar: Voltage Regulators	$T_A \geq 125$ °C V_{out}= Terminated to ground through R_L	Not required	ΔI_{SCD} ΔV_{OUT}	**DC**: I_{CC}, V_{OUT}, I_{OS}, line/load regulation
Linear Bipolar: Pulse-width-modulator	Not required	$T_A \geq 125$ °C V_{out}= Terminated to ground through R_L R_{ext}, C_{ext} connected if applicable.	ΔI_{IO} ΔV_{REF}	**DC**: V_{REF}, I_{IB}, I_{IO}, I_{OS}, V_{IO}, V_{OL}, V_{OH}, A_V, CMRR, PSRR **AC**: T_R , T_F, f_{OSC}
Darlington Transistor Array	$T_A \geq 125$ °C V_{out}= 15 Vdc through R_L	Not required	ΔI_{CEX} Δh_{FE}	**DC:** $V_{CE(SAT)}$, V_F, I_{CEX}, I_F **AC**: h_{FE}, t_{PHL}, t_{PLH}
Linear CMOS Timers	$T_A \geq 125$ °C $V_{out} = V_{CC}$ through R_L	Not required	ΔI_{CEX} ΔV_{OH} ΔV_{OL}	**DC**: V_{TRIG}, V_{TH}, V_R, V_{OL}, V_{OH}, V_{SAT}, I_{CC}, I_{TRIG}, I_{TH}, I_R, I_{CEX} **AC**: T_{TLH}, T_{THL}

See notes on page C-35.

Table 10A Burn-In and Electrical Measurement Requirements for Monolithic ICs (Page 3 of 4)

IC Type	Required Burn-In (Note 4)		Delta	Electrical Measurement (Notes 1, 2, 3)
	Static (Condition C)	**Dynamic (Condition D)**		
Linear MOS and Bipolar: Active Filters	Not required	$T_A \geq 125$ °C V_{in}= Sine wave at Frequency < f_O V_{out}= Terminated to ground through R_L	ΔI_{CC} ΔV_{OS}	**DC**: I_{CC}, I_{SS}, V_{OS} **AC**: f_O, Q, input frequency range
Mixed Signal MOS, Bi-CMOS and Bipolar: (Note 7) Analog to Digital (A/D) Converters.	$T_A \geq 125$ °C V_{in} = Max analog dc input $V_{out} = V_{CC}/2$ through R_L	$T_A \geq 125$ °C V_{in}= Analog input to generate maximum digital codes. $V_{out} = V_{CC}/2$ through R_L	ΔI_{CC} ΔI_{EE} ΔV_{IO}	**DC**: V_{REF}, V_{OH}, V_{OL}, V_{IO}, I_{CC}, I_{EE}, I_{IL}, I_{IH}, I_{OZL}, I_{OZH}, I_{OS}, Zero Error, Gain Error, Linearity Error. **AC:** T_C, T_S, T_H **Functional Test:** Verify codes
Mixed Signal MOS, Bi-CMOS and Bipolar (Note 7) Digital to Analog (D/A) Converters.	$T_A \geq 125$ °C $V_{in} = V_{DD}$ on one-half data inputs and V_{SS} on remaining inputs. V_{out}= Terminated to ground thru R_L	$T_A \geq 125$ °C V_{in} = Apply appropriate digital codes for all inputs and for control signals. V_{out} = Terminated to ground through R_L.	ΔI_{CC} ΔI_{EE}	**DC**: I_{CC}, I_{EE}, I_{IL}, I_{IH}, I_{OZL}, I_{OZH}, I_{OS}, Zero Error, Gain Error, Linearity Error, PSRR **AC:** T_C, T_S, T_H **Functional Test:** Verify codes

Notes:

1. See MIL-S-1331 for symbol definitions.
2. These are typically recommended electrical parameters. Since electrical parameters are device dependent, refer to detail specifications for actual DC and AC parametric test conditions and limits.
3. For digital devices, all DC parameters, functional tests, and switching tests shall be tested at 25°C, at minimum operating temperature and at maximum operating temperature. AC tests (e.g C_{IN}) are tested initially and after any design or process changes.

   For linear devices, all DC parameters shall be tested at 25°C, at minimum operating temperature and at maximum operating temperature. All AC and switching tests shall be performed at 25°C.
4. Static and Dynamic burn-in shall be performed at maximum recommended operating supply voltage with V_{in} and R_L selected to assure that the junction temparature shall not exceed T_{jmax} specified for the device type.
5. For one-time programmable devices, (e.g. PROMs, PALs and FPGAs) dynamic burn-in shall be performed on programmed devices with user application specific burn-in circuit. The post burn-in should include DC, AC, and functional tests for user's program verification.
6. Dynamic burn-in required for Grade 2 parts.
7. Static or dynamic burn-in acceptable for Grade 2 parts.

Table 10B Hybrid Integrated Circuit Screening Requirements

Inspection/ Test	Methods	MIL-STD-883 Conditions and Requirements	Grade 1	Grade 2
1. Pre-seal Burn-in	1030		Optional	Optional
2. Nondestructive Bond Pull	2023	PDA ≤ 2% or 1 wire.	X	
3. Internal Visual	2017	Condition A or B. (Note 1)	X	X
4 Stabilization Bake	1008	Condition C	X	X
4. Temperature Cycling	1010	Condition B (-55 °C to +125 °C) for 10 cycles	X	X
5. Constant Acceleration	2001	Condition A Y_1 orientation only	X	X
6. PIND	2020	Condition A or B.	X	X
7. Radiographic	2012	Can be performed at any sequence after PIND.	X	
8. Serialization			X	
9. Initial Electrical Measurements		Electrical measurements and delta parameters are done per applicable device specification (Note 2).	X	X
10. Burn-In	1015	Condition A, B, C, or D @ $T_A \geq 100$ °C. Duration (hours) for Static /Dynamic burn-in (Note 2, 3).	X 160/160	X 160
11. Final Electrical Measurements		For Grade 1, interim electrical tests shall be performed after the first 160-hour burn-in.	X	X
12. Calculate Deltas		Per applicable device specification	X	
13. Calculate PDA		PDA applies to selected DC tests and delta for Grade 1 during the second burn-in only.	Δ+DC ≤ 2%	DC ≤ 10%
14. Hermetic Seal a. Fine Leak b. Gross Leak	1014	 Condition A or B Condition C	X	X
15. External Visual	2009	3 X to 10X	X	X

Notes:

1. Destructive Physical Analysis may be performed to the requirements of S311-M-70 in lieu of internal visual for devices used in Grades 2.
2. Burn-in and electrical measurements are not included for hybrids due to many customer designs and many different functional configurations; they shall be specified in the detail specifications or altered item drawings.
3 For Grade 1 parts, the burn-in period shall be divided into two successive 160- hour minimum burn-in; included in that total 320-hour time may be a combined static and dynamic configurations. For Grade 2 parts, only one burn-in is required, and it can be either static mode or dynamic mode.